Integration of III-V Materials on Silicon Substrates for Multi-junction Solar Cell Applications

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Abstract—**The work presented here aims to reduce the cost of multijunction solar cell technology by developing ways to manufacture them on cheap substrates such as silicon. In particular, our main objective is the growth of III-V semiconductors on silicon substrates for photovoltaic applications. The goal is to create a GaAsP/Si virtual substrates onto which other III-V cells could be integrated with an interesting efficiency potential. This technology involves several challenges due to the difficulty of growing III-V materials on silicon. In this paper, our first work done aimed at developing such structure is presented. It was focused on the development of phosphorus diffusion models on silicon and on the preparation of an optimal silicon surface to grow on it III-V materials.**

Keywords—III/V on Si heteroepitaxy, Metal-Organic Vapor Phase Epitaxy (MOVPE), metamorphic, multi-junction solar cell.

I. INTRODUCTION

Multi-junction solar cells are the most promising devices to attain highly efficient solar energy conversion into electricity. These devices are formed by stacks of several sub-cells series connected by tunnel junctions, each of one transforming optimally a portion of the solar spectrum into electrical energy. Due to this optimized use of the solar spectrum, the maximum conversion efficiency which can be achieved by a multi-junction solar cell with an infinite number of junctions is more than twice that reached with a single p/n junction [1]. The keys to the success of this technology are 1) the use of III-V semiconductors (a family of materials with excellent photovoltaic (PV) properties and a wide range of suitable band gaps to implement multi-junction solar cells) and 2) the existence of a high-quality industrially mature crystal growth technology called Metal-Organic Vapour Phase Epitaxy (MOVPE) specially suited for the epitaxial growth of such III-V semiconductors.

The heteroepitaxial growth of III-V semiconductors on germanium by MOVPE has been successfully developed in the last two decades. Although a multi-junction solar cell using this material as substrate has beaten the efficiency record for any photovoltaic device, achieving an efficiency close to 42% [2], the use of alternative substrates to Ge comes up as a result of the shortage and elevated costs of this material. Obviously, the goal is that the new substrates circumvent the limitations of Ge, i.e. are inexpensive and abundant [3]. Accordingly, the ideal candidate is silicon, the ubiquitous electronic and photovoltaic material. The growth of III-V semiconductors on Si has been a long-sought desire by the microelectronic industry [4]. Particularly, in the PV field, the integration of III-V compounds on Si was intensively investigated in the 1990s, achieving good results [5]. However, the intensity of this research declined considerably in the late 1990s due to the difficulty in improving material quality and reproducibility.

In this paper we propose a solar cell design based on III-V metamorphic materials grown on silicon and the first theoretical and experimental studies for its implementation.

II. SOLAR CELL DESIGN

The work presented here is focused on investigating the epitaxial growth of III-V semiconductor materials on silicon with sufficient photovoltaic quality for their eventual integration into multijunction hybrid III-V/silicon solar cells.

Figure 1, adapted from [6], shows the theoretical efficiencies reachable with a dual-junction solar cell (DJSC) as a function of the sub-cells band gap. Figure 1 makes evident that GaP is not a suitable material for the top cell due to its large band gap (2.2 eV), despite the fact that it seems to be the ideal candidate concerning its lattice constant, which is close to that of Si. For that reason, a top cell material with an ideal band gap (1.66 eV) is needed, which can be achieved by adding arsenic to GaP to produce $GaAs_{1-x}P_x$, obtaining an interesting efficiency potential (theoretical limit above 40%).

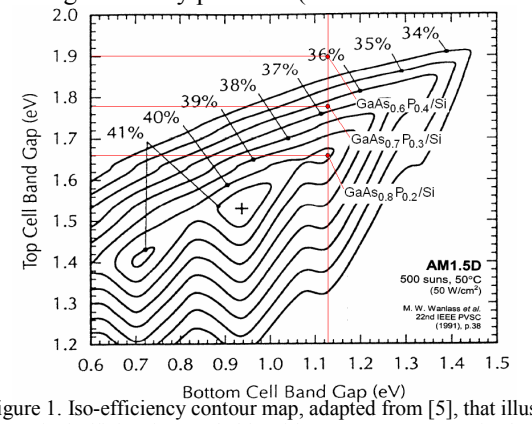

Figure 1. Iso-efficiency contour map, adapted from [5], that illustrates the theoretical efficiencies reachable with a DJSC grown on Si. The efficiency potential for $GaAs_{1-x}P_x$/Si cells for three different compositions is included.

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The use of III/V compounds has been widely studied for growing different solar cell structures. In 1995, Soga et al. achieved a record efficiency of about 20% AM0 [5] with a tandem solar cell based on AlGaAs/Si, using thermal cycle annealing (TCA) to allow the relaxation of the material. This technology has also produced excellent results in growing GaAsP on GaAs substrates [7]; however, it has been proved that the use of Si substrates involves much greater challenges, achieving efficiencies of only 9.2% AM0 for a tandem $GaAs_{0.7}P_{0.3}$ / Si solar cell using TCA [8].

Our first objective is to grow a first GaP nucleation layer on silicon (which have similar lattice constants) in order to grow on them metamorphic $GaAs_{1-x}P_x$ buffer layers with variable arsenic content onto which the top cell can be easily integrated (Fig. 2). A metamorphic material is one grown on a substrate with a different lattice constant in a way that its relaxation is promoted, mainly through the occurrence of misfit/threading dislocations at the interface.

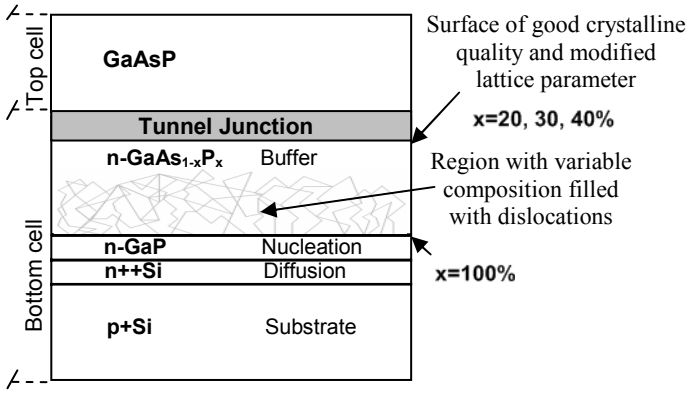

Figure 2. Structure of a dual-junction $GaAs_{1-x}P_x$/Si solar cell

Our proposed is to investigate buffer layers with a final phosphorus content of 20%, 30% and 40% to implement three variants of the multi-junction solar cell, in order to find the optimum trade-off between the best band gap and the lowest density of structural defects. The purpose of the buffer layer is to make an optimal transition between the nucleation layer and the top cell, so if we can minimize the vertical propagation of defects, once total relaxation is obtained, the resulting top surface will have the desired lattice constant and good crystalline quality (this is what is called a virtual substrate). This technique has been widely used in the growth of III-V materials on germanium, where it has been demonstrated that it is possible to engineer the lattice constant and still maintain the good crystalline quality needed for a high photovoltaic performance [9].

III. BASIC MOVPE PROCESS

The epitaxial growth of the structure depicted in figure 2 involves several challenges. However, based on the wide experience accumulated on other group IV substrates −namely germanium− a general overview of the MOVPE process can be given. Figure 3 schematically shows such overview, by plotting the time evolution of the temperature and the flows of the main precursors used during the growth.

As shown by figure 3, just after the wafers are loaded into the reactor, the temperature is raised to a high value (T>850ºC) to promote a thermal cleaning of the substrate. The goal of such "heat bake" is to force the pyrolysis and/or direct evaporation of the native oxide and any possible adsorbates on the substrate surface. In the case of silicon oxide, temperatures over 1000ºC are needed for its thermal decomposition. However, lower temperatures (~850ºC) can be used if specific chemical cleanings [10] are applied just prior loading the wafers into the reactor.

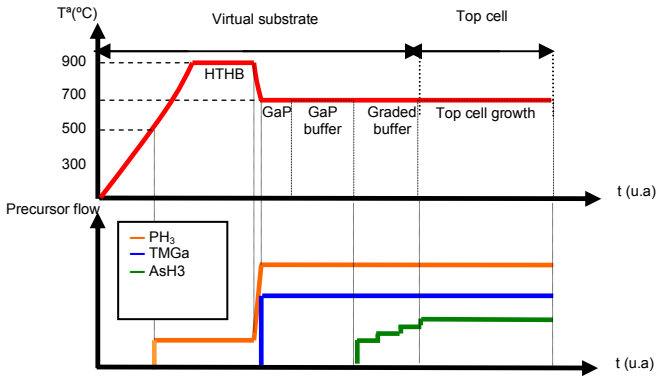

Figure 3. Evolution of different growth parameters during the DJSC growth

As figure 3 shows, this high temperature heat bake is performed under a small PH_3 flow. The reason for this is to control the evolution of the substrate surface prior to growth. In our case, the ideal surface configuration consists of a set of silicon terraces of uniform width fully covered by phosphorus dimmers forming a single domain surface (all dimmers oriented coherently with respect to step edges) and separated by double steps. Such configuration is ideal since it has been demonstrated to prevent the formation of antiphase domains and twins, the ubiquitous defects in III-V on IV heteroepitaxy [11]. Thus, the goal of this flow of PH_3 is to act as a controlled supply of P to induce the desired surface reconstruction and to provide some atomic hydrogen to aid the elimination of the oxide. In this step, due to the high temperatures reached, the phosphorus begins the diffusion into the silicon substrate creating the emitter of the silicon sub-cell (n-type region). During that step, the overpressure of phosphine has to be high enough to compensate the desorption of the V-group elements that are present in a MOVPE reactor (walls and susceptors) and which can be harmful for silicon (i.e. As).

The following step would be the growth of a few nanometers of GaP on the silicon substrate. Once the first mono-layers have been epitaxially grown, we will have a perfect GaP surface onto which the GaP buffer could be grown. Finally, the GaAsP graded buffer will be grown on the GaP layer, by introducing trimethylgallium, phosphine and increasing flows of arsine in the reactor.

In this work we have first focused on the modelling of the formation of the Si sub-cell by the diffusion of group V atoms during the growth of the nucleation layer. The optimization of the pre-nucleation routine has also been studied to ensure that the substrate is prepared for a heteroepitaxy in the best conditions. Once the routine to create GaAsP/Si virtual substrates is optimized, it will be possible to undertake the set of experiments intended to calibrate the growth of the materials needed for a first implementation of the GaAsP top cell in the tandem GaAsP/Si and the tunnel junction between both sub-cells.

IV. DOPANT DIFFUSION MODELS FOR SILICON

As mentioned in the previous section, the use of PH_3 and high temperatures at the beginning of the MOVPE process causes the diffusion of P into the Si substrate and the subsequent formation of the emitter of the Si bottom sub-cell of the multi-junction solar cell. The emitter thickness achieved is controlled by a two-step process. First, an initial phosphorous diffusion is carried out during the heat bake as a consequence of the high temperatures reached (850ºC during 30-40 min) and due to the presence of a virtually unlimited supply of P dimmers on the surface. This is followed by a second diffusion step associated to the thermal load suffered by the structure during the rest of the MOVPE process (675ºC during 3-4h) that pushes the diffused phosphorus deeper into the substrate. This situation conforms a process slightly different to conventional P diffusion in state-of-the-art PV technology.

In order to have a first estimation of the emitter P profile and thickness (and thus calculate the internal quantum efficiency of the bottom sub-cell), different P diffusion profiles have been simulated for a 10^{16} cm^{-3} p-type Si wafer, as a function of the temperature and the diffusion time [12]. These simulations have been carried out considering an unlimited phosphorus supply during the whole process and without taking into account the influence of other parameters in the P diffusion, associated to the work conditions in the MOVPE reactor (i.e. possible impact of atomic hydrogen). These simulations allowed us to estimate the upper limit of the emitter thickness, since the profiles presented here have been calculated for a specific and constant temperature during the whole process and considering an unlimited source (Fig. 4).

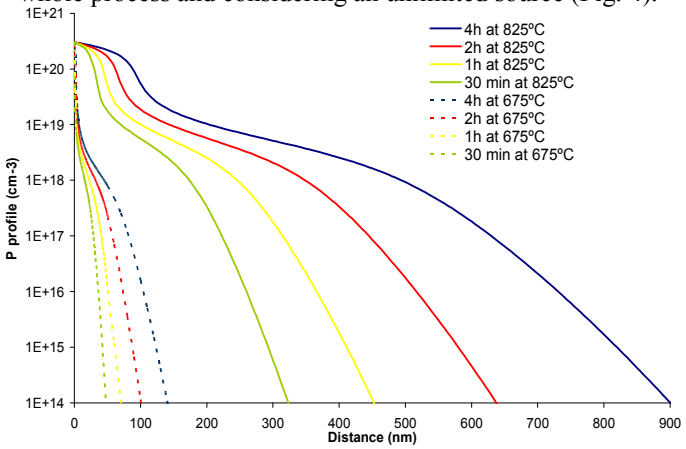

Figure 4. Diffusion profiles for Phosphorous in silicon for 675ºC and 825ºC

From these P profiles we can conclude that the diffusion process originated during the heat bake, will contribute more to the Si sub-cell emitter formation than the drive-in process. The emitter thickness, under these conditions will be in the range of hundreds of nanometers (~500 nm), which is relatively thin compared to the whole silicon sub-cell thickness and much lower than the one usually obtained in conventional silicon PV technology. This fact determines the internal quantum efficiency (QE) of these sub-cells. Figure 5 shows the simulated bottom-cell QE efficiency for the different P diffusion profiles at 825ºC, as a function of the diffusion time. The wavelengths corresponding to the band gap of three different top cell configurations are depicted.

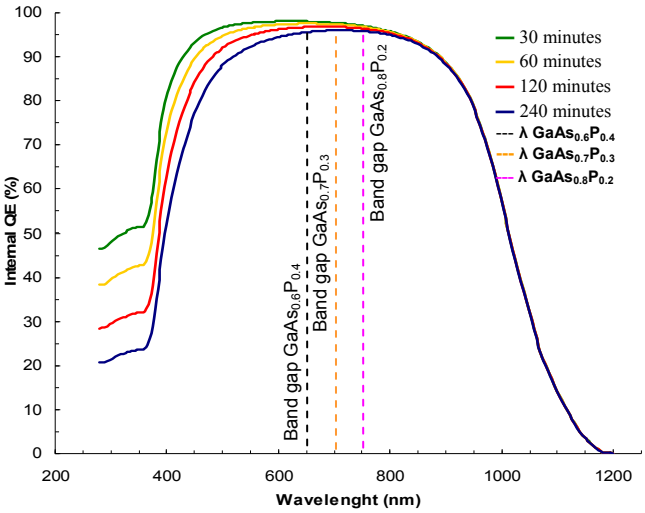

Figure 5. Bottom cell internal QE for P-in-Si diffusion profiles at 825ºC. Top cell band gap is depicted for three different configurations.

According to these simulations, the lower-wavelength region of the device QE is affected by the high P concentrations in the emitter, which clearly decreases the minority carrier lifetime in that region. If the Si cell were working as a single-junction solar cell, shallower diffusions would be desirable to raise the emitter contribution to the cell QE. Fortunately, in a tandem stack only the high-wavelength part of the spectrum reaches the bottom sub-cell. For that low-energy radiation, the cell QE is basically independent of the P diffusion depth. Furthermore, as it is also shown in figure 5, the configuration of the top cell does not involve an important variation in the QE. Thereby, the bottom cell base (i.e. the p-type substrate) is expected to be responsible for the photovoltaic optical performance of the bottom sub-cell in the tandem stack, since it is not expected that the MOVPE environment introduces a significant amount of lifetime killing impurities into the wafer.

V. FIRST HETERONUCLEATION EXPERIMENTS

Some experimental studies have also been carried out in order to determine the conditions that ensure an optimal Si surface to epitaxially grow III-V materials. It is well known that in order to ensure an optimal substrate, it is necessary to remove the native Si oxide either by thermal desorption above 1000ºC or by chemical etching, based on the method proposed by Ishizhaka and Shiraki [10]. To avoid a possible contamination of EPI-ready wafers (i.e. prepared for epitaxial growth), with particles from the chemical etch and since this process could be time-consuming and expensive, we first examined the possibility to perform an *in situ* cleaning of the substrates under hydrogen/hydride atmosphere. The goal was to remove the native oxide assisted by atomic hydrogen resulting from the pyrolysis of PH_3 at high temperatures. With this goal, Si substrates were baked at 750ºC (due to the impossibility to reach higher temperatures in our current MOVPE reactor) under different PH_3 flows for different times in a MOVPE environment, and then a few nanometers of GaP were grown.

Samples were characterized using transmission electron microscopy (TEM) operating at an acceleration voltage of 200 KV. Cross-section TEM samples were prepared by mechanical polishing followed by Ar^+ -ion milling.

From the TEM characterization it has been observed that, in all samples, GaP has grown in a polycrystalline island-type. These islands have grown with a non-uniform distribution, showing different sizes and forms (Fig. 6). From the high resolution images it can be observed that the surface preparation of EPI-ready wafers by *in situ* pretreatment in H_2/PH_3 atmosphere has not been successful, since a remaining Si oxide layer is still present on the surface (Fig. 7a). Moreover, many dislocations, twins and defects inside the islands can be observed, as well as clear grain boundaries (Fig. 7b).

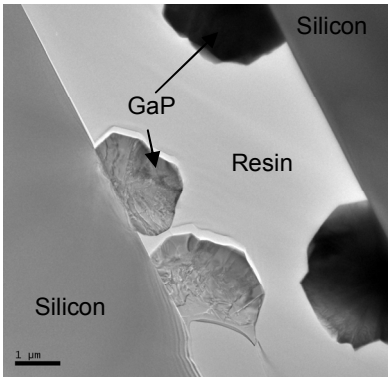

Figure 6. GaP island-type growth on as received Si EPI-ready substrates

Once checked that thermal desorption at current MOVPE conditions was not successful in removing the native oxide, the suitability of chemical cleaning of wafers before being loaded into the reactor was analyzed. Heteroepitaxial growth of a thin GaP layer was carried out on a chemically cleaned Si wafer following the Ishizhaka and Shiraki method. Promising results based on the appearance of reflectance anisotropy signal (RAS) and on macroscopic observations have been pointed out. TEM observations of these samples are ongoing.

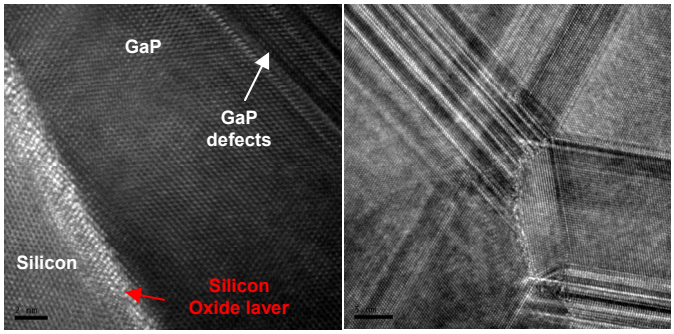

Figure 7. HRTEM images of a polycrystalline GaP-island where silicon oxide layer still remained (7a) and grain boundaries were revealed (7b).

VI. CONCLUSIONS

Despite the huge potential of heteroepitaxial growth of III-V semiconductors on Ge by MOVPE, the use of alternative substrates arises as a consequence of the limitations of Ge. In this paper, we have proposed a challenging metamorphic DJSC design based on a GaAsP/Si structure, with a theoretical efficiency up to 40% (much higher than the one reached with AlGaAs/Si tandem solar cells). First, by dopant diffusion models, the thickness and the PV quality of the bottom cell emitter created by the P diffusion has been studied. The simulations show that the emitter will be relatively thin compared to thickness of the whole silicon sub-cell, reason why the cell QE will be basically independent of the P diffusion depth. It has also been proved that the configuration of the top cell will not play an important role in the cell QE. Thus, the PV quality of the device will be determined by the base of the bottom cell. In addition, some studies have been carried to determine the conditions that ensure an optimal silicon surface for heteroepitaxial growth. It has been proven, by TEM observations, that *in-situ* pretreatment under H_2/PH_3 atmosphere is not suitable for obtaining a Si oxide-free surface. Therefore, chemical cleaning of wafers following the Ishizaka and Shiraki method has been performed before loading wafers into the reactor, showing promising results. TEM analysis of these samples is ongoing.

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